EM Injection Vs. Modern CPU

Fault Characterization and AES Differential Fault Analysis

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Digital system usage

- Secure elements
- ✓ Certified

- High-performance component
- ✗ Not fully certified

Both are powered by System On Chips (SoCs)

System On Chip differences

Secure element

- simple CPU
- few modules
- internal memory only
- few communication interfaces

➔ Small attack surface

High-performance component

- complex CPU
- multiple modules
- internal and external memory
- multiple interfaces

➔ Large attack surface

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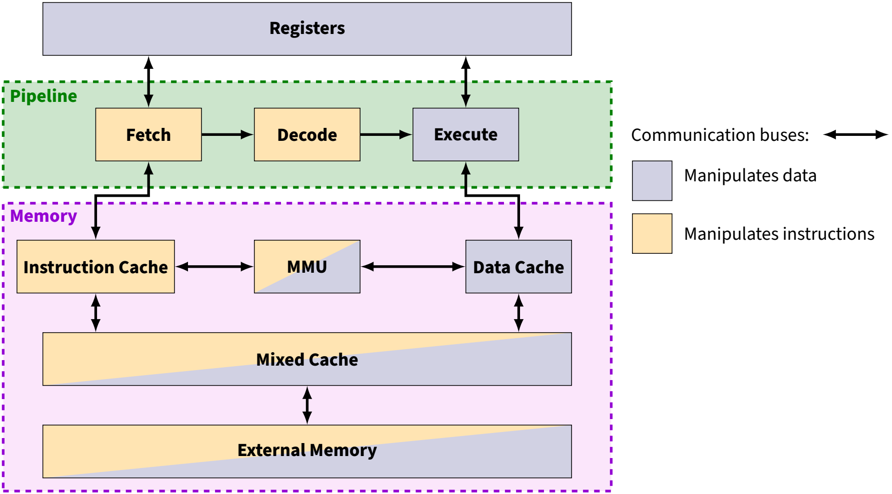
Focus on the Modern CPU **behaviour against** Fault Injections **attacks**

Complex CPU modelling overview

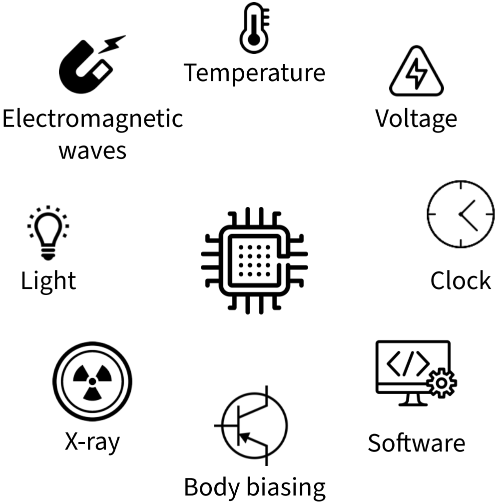
A CPU can be simplified as a set of modules:

1. A pipeline which fetches, decodes and executes instructions
2. Registers where manipulated data are temporarily stored
3. A memory to store instructions and data

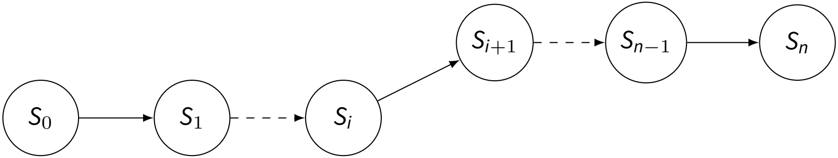
Complex CPU modelling overview (cont.)



When the hardware is perturbed ...



… the software gone wild



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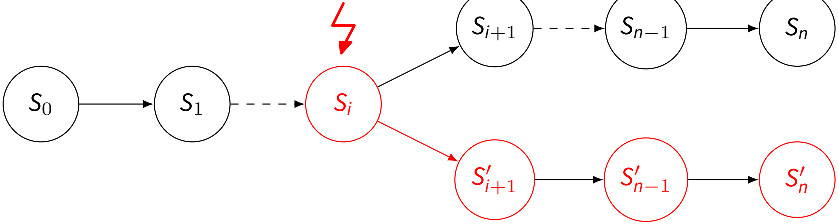


Overview of the fault effect characterization

Injection mediums

Abstraction layer

	Clock	Voltage	EM	Laser
Program				
ISA				
Micro-architecture				

Legend: MCU's CPU SoCs' CPU FPGA Our work

Overview of the fault effect characterization

Injection mediums

Abstraction layer	Clock	Voltage	EM	Laser
Program		Forced memory ACK on MCUs [BFP19]	Control flow hijacking on ARM Cortex-M3 [BLLL18]	
ISA	Instruction skip and corruption on ATMega163 [BGV11]		Data corruption on ARM Cortex-M3 [MHD$^+$14] Instruction skip on ATMega328P [MDP$^+$20]	Instruction skip and data corruption on ATMega328P [BJ15]
ISA / Micro-architecture	Data and instruction corruption on MCUs [KH14]	Data and instruction corruption on MCUs [KH14]		
Micro-architecture	Pipeline corruption on RISC-V LEON-3 [YGS15]		Cache corruption on ARM Cortex-M4 [RNR$^+$15] Data bus corruption [MDH$^+$14] on ARM Cortex-M3 Flash corruption on MCUs [bec19, MBD$^+$19]	Flash corruption on ATMega328P [KBB$^+$18] and ARM Cortex-M3 [CMD$^+$19]

Legend: MCU's CPU | SoCs' CPU | FPGA | Our work

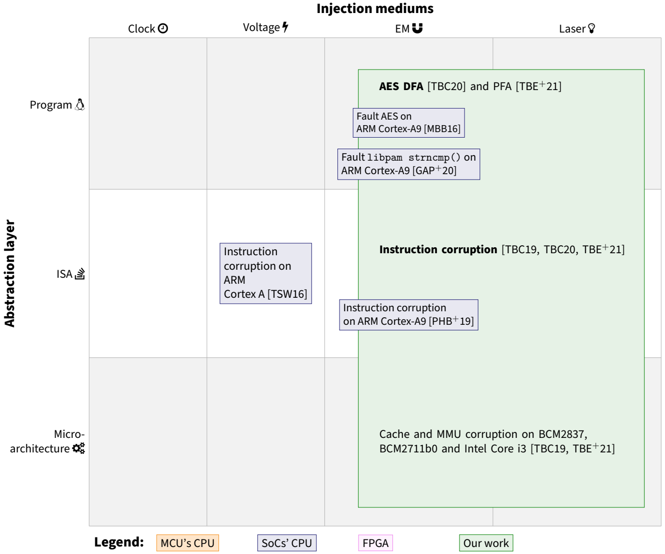
Overview of the fault effect characterization

Injection mediums

Abstraction layer	Clock	Voltage	EM	Laser
Program			Fault AES on ARM Cortex-A9 [MBB16] Fault `libpam strncmp()` on ARM Cortex-A9 [GAP+20]	
ISA		Instruction corruption on ARM Cortex A [TSW16]	Instruction corruption on ARM Cortex-A9 [PHB+19]	
Micro-architecture				

Legend: MCU's CPU SoCs' CPU FPGA Our work

Overview of the fault effect characterization



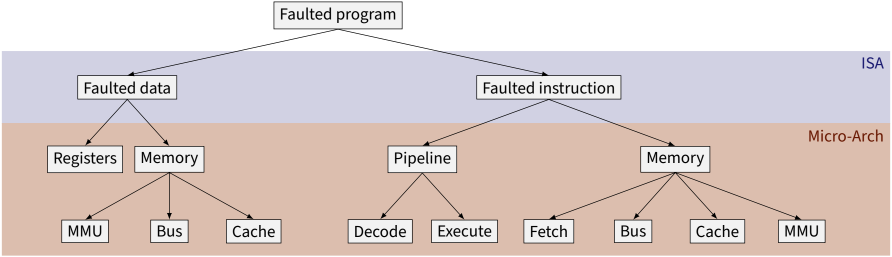
Fault effects analysis on complex CPU

During a fault, a least one micro-architectural block is perturbed

Modus operandii [TBC19]

- A test program is faulted during its execution
- Faulting various test program gives information about the micro-architectural behaviour.

Fault effects analysis on complex CPU (cont.)



Characterization Method

Test program 1

```
mov r3, r3;
/*
 * Arbitrary number
 * of repetitions
 */
mov r3, r3;
```

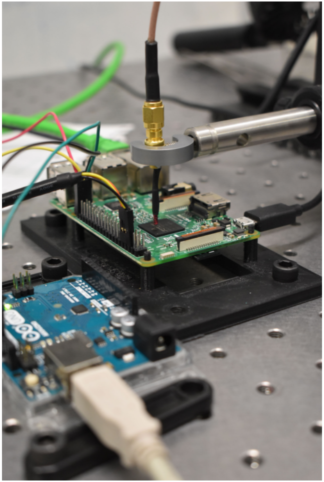
Test program 2

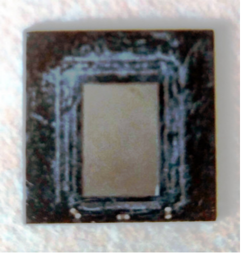
```
orr r3, r3;
/*
 * Arbitrary number
 * of repetitions
 */
orr r3, r3;
```

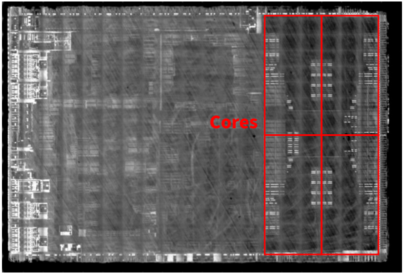
Initial values

Register	Initial values
r0	0xfffe0001
r1	0xfffd0002
r2	0xfffb0004
r3	0xfff70008
r4	0xffef0010

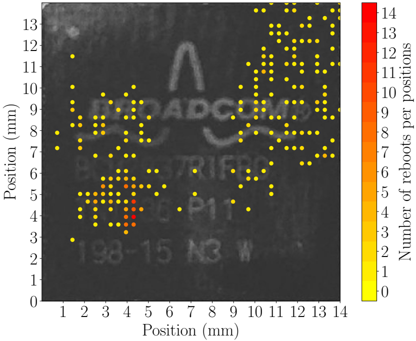
Characterization - BCM2837 (Raspberry Pi 3)



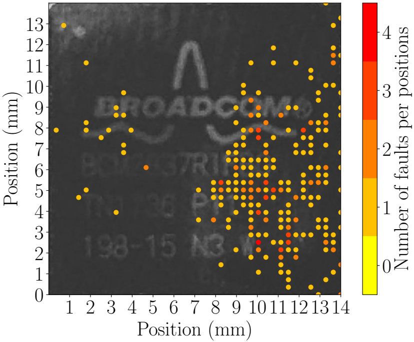




Characterization - BCM2837 (Raspberry Pi 3)



Spots leading to reboots

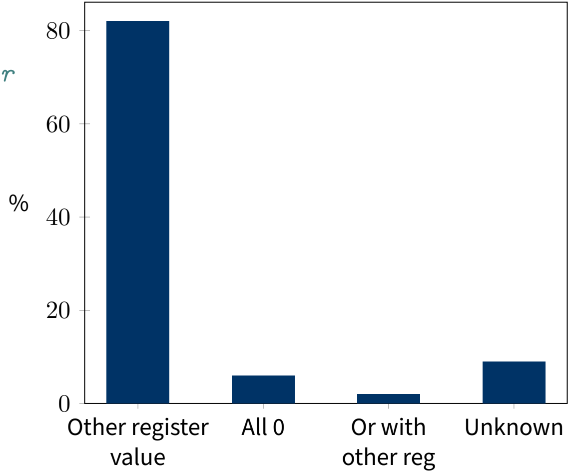


Spots leading to faults

Fault analysis on program 1

```
mov r3, r3;
/*
 * Arbitrary number
 * of repetitions
 */
mov r3, r3;
```

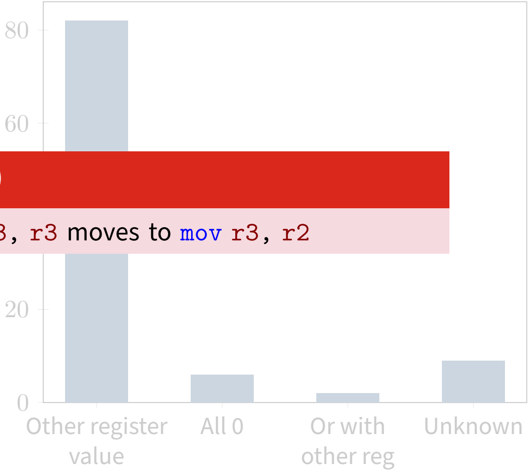
Register	Initial values
r0	0xFFFE0001
r1	0xFFFD0002
r2	0xFFFB0004
r3	0xFFF70008
r4	0xFFEF0010



Fault analysis on program 1

```
mov r3, r3;
/*
 * Arbitrary number
 * of repetitions
 */
mo
```

Regist	
r0	0xFFFE0001
r1	0xFFFD0002
r2	0xFFFB0004
r3	0xFFF70008
r4	0xFFEF0010



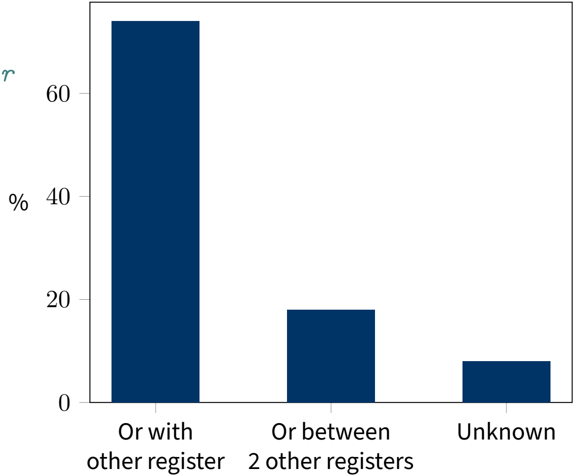
Most of time (80%)

The instruction `mov r3, r3` moves to `mov r3, r2`

Fault analysis on program 2

```
orr r3, r3;
/*
 * Arbitrary number
 * of repetitions
 */
orr r3, r3;
```

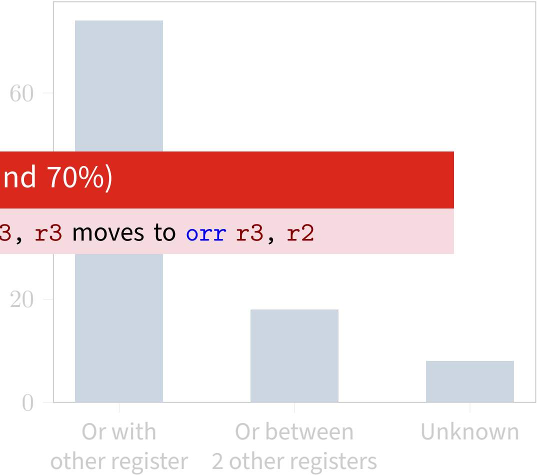
Register	Initial values
r0	0xFFFE0001
r1	0xFFFD0002
r2	0xFFFB0004
r3	0xFFF70008
r4	0xFFEF0010



Fault analysis on program 2

```
orr r3, r3;
/*
 * Arbitrary number
 * of repetitions
 */
or
```

Regist	
r0	0xFFFE0001
r1	0xFFFD0002
r2	0xFFFB0004
r3	0xFFF70008
r4	0xFFEF0010



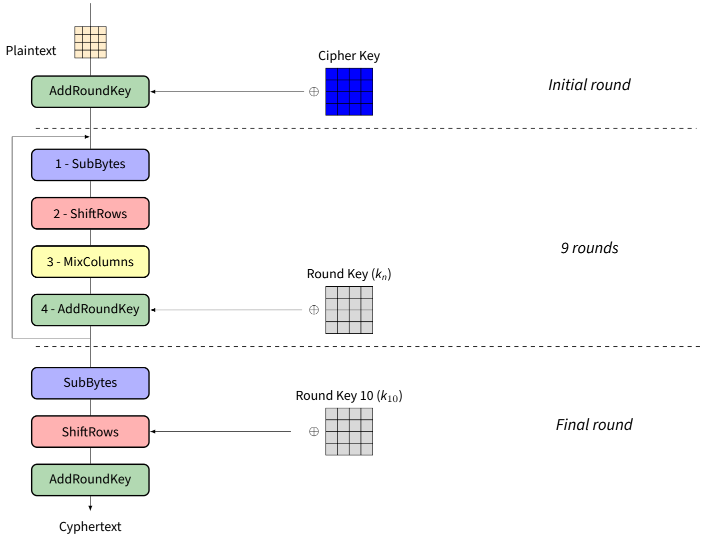
Most of time (around 70%)

The instruction `orr r3, r3` moves to `orr r3, r2`

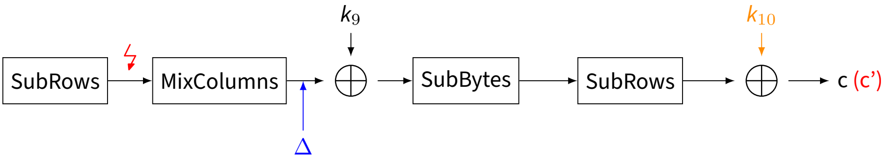
Results

- Different instructions are similarly modified
- Most of time, the second operand moves to `r2`
- Can we exploit it?

Advanced Encryption Standard (AES)

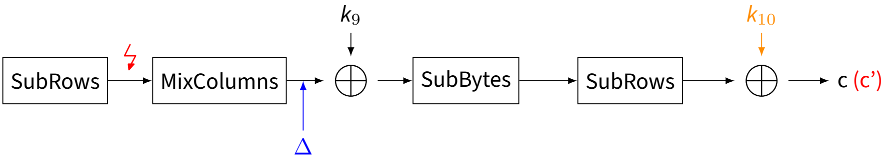


Exploitation – Differential Fault Analysis (DFA)



$$\Delta = SB^{-1}(SR^{-1}(c \oplus k_{10})) \oplus SB^{-1}(SR^{-1}(c' \oplus k_{10}))$$

Exploitation – Differential Fault Analysis (DFA)



$$\Delta = SB^{-1}(SR^{-1}(c \oplus k_{10})) \oplus SB^{-1}(SR^{-1}(c' \oplus k_{10}))$$

Setup

- OpenSSL implemention for Debian 9 on RaspberryPi3
- EMFI medium

Results

We made 3000 injections (around 1-hour required) and obtained 466 faults (15.54%):

- Only 16 (4.348%) have only one diagonal faulted => fault the cipher
  - Only 8 (50%) correspond to one byte fault before the `MixColumns` operation

Results

We made 3000 injections (around 1-hour required) and obtained 466 faults (15.54%):

- Only 16 (4.348%) have only one diagonal faulted => fault the cipher
  - Only 8 (50%) correspond to one byte fault before the `MixColumns` operation

- A suitable faulted cipher for the DFA occurs each 1/234 cipher (0.34%)
- If an injection requires 2 secondes => a suitable cipher is obtained is 10 minutes
- 3 hours of injection are needed to completely obtain to achieve the exploitation

Conclusion and future works

- From fault model analysis to exploitation
- What about fault model from ISA to complex software layout
  - Ongoing work on `sudo` program
- Reproduction-setup problem?

Questions?

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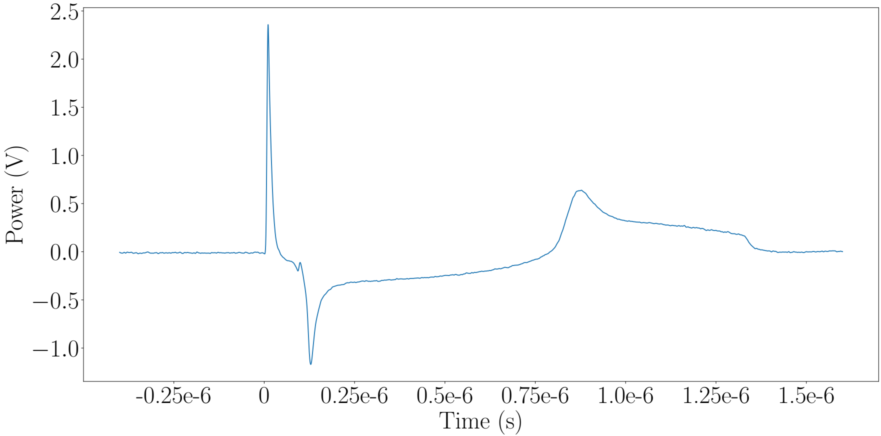
EM injector

EM injector

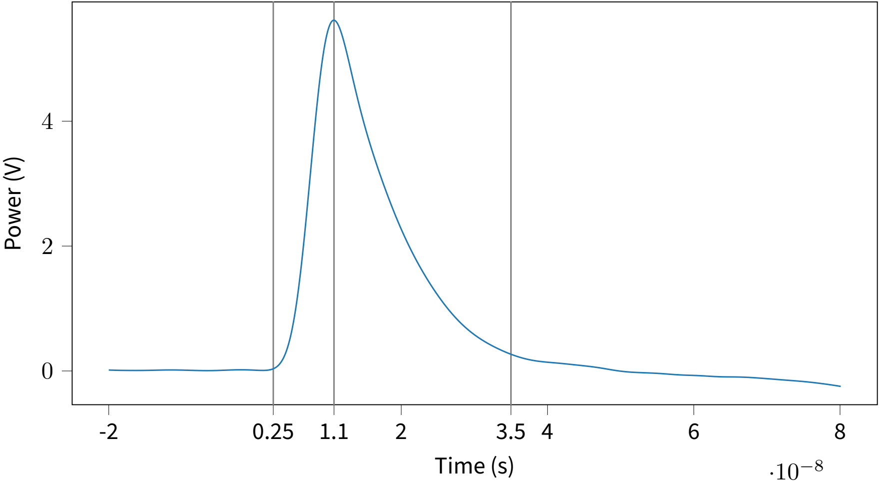
AvTec pulse generator → max 800 V/16 A



Pulse generated by the AvTech (100 V input)

EM injector

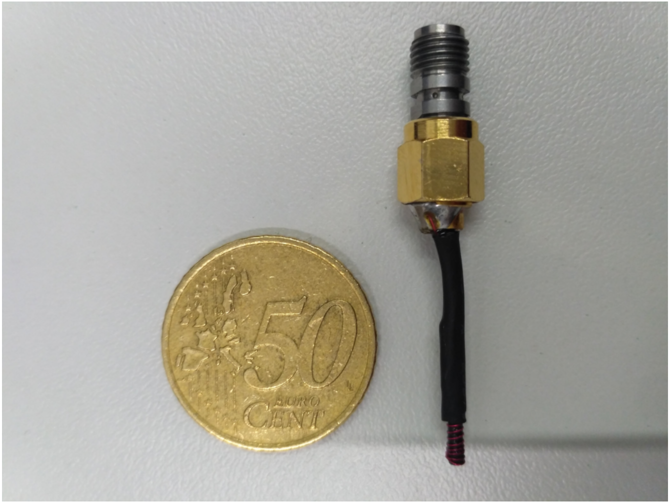
AvTec pulse generator ➞ max 800 V/16 A



Pulse generated by the AvTech zoomed on the first peak (200 V input)

EM Probe

- Home-made EMFI probe



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